University of Dayton

ECE

Mumma Radar Lab

Comprehensive VHDL

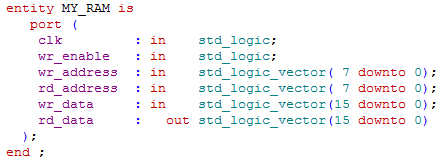
Fall 2016

Homework 5

Memory Design

In this homework, you will design a 255 deep by 16 bits width RAM [look at the PPT example]

Here is the design entity:



Make sure your TB is self-checking.